

ABSTRACT OF THE DISCLOSURE

A microprocessor is configured to fetch a compressed
5 instruction set which comprises a subset of a corresponding
non-compressed instruction set. The compressed instruction
set is a variable length instruction set including 16-bit
and 32-bit instructions. The 32-bit instructions are coded
using an extend opcode, which indicates that the instruction
10 being fetched is an extended (e.g. 32 bit) instruction. The
compressed instruction set further includes multiple sets of
register mappings from the compressed register fields to the
decompressed register fields. Certain select instructions
are assigned two opcode encodings, one for each of two
15 mappings of the corresponding register fields. The
compressed register field is directly copied into a portion
of the decompressed register field while the remaining
portion of the decompressed register field is created using
a small number of logic gates. The subroutine call
20 instruction within the compressed instruction set includes a
compression mode which indicates whether or not the target
routine is coded in compressed instructions. The
compression mode is stored in the program counter register.
The decompression of the immediate field used for load/store
25 instructions having the global pointer register as a base
register is optimized for mixed compressed/non-compressed
instruction execution. The immediate field is decompressed
into a decompressed immediate field for which the most
significant bit is set.

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